Amendments to the Claims:

The listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of Claims:

1-15. (Cancelled)

16. (Previously Presented) A dual damascene interconnection structure with a metal-insulator-metal capacitor, the structure comprising:

a via-level intermetal dielectric and a trench-level intermetal dielectric which are sequentially stacked on a substrate;

a dual damascene interconnection formed in the via-level intermetal dielectric and the trench-level intermetal dielectric including a line trench extending through the trench-level intermetal dielectric to the via-level intermetal dielectric;

a metal-insulator-metal capacitor formed between the via-level intermetal dielectric and the trench-level intermetal dielectric to include a lower electrode, a dielectric layer, and an upper electrode, the dual damascene interconnection being substantially electrically isolated from the metal-insulator-metal capacitor; and

an upper metal interconnection formed on and connected to the upper electrode.

17. (Previously Presented) The structure of claim 16, further comprising:

a first lower metal interconnection and a second lower metal interconnection, which are formed between the substrate and the via-level intermetal dielectric; and

a via which is included in the via-level intermetal dielectric to connect the lower electrode and the first lower metal interconnection;

wherein the dual damascene interconnection is connected to the second lower metal interconnection.

18. (Original) The structure of claim 17, wherein the first lower metal interconnection and the second lower metal interconnection are damascene interconnections buried in an insulating layer formed on the substrate.

19. (Original) The structure of claim 17, wherein the via is filled in a hole-type opening.

20. (Original) The structure of claim 17, wherein the via is filled in a line-type opening.

21. (Original) The structure of claim 16, wherein the lower electrode, the dielectric layer, and the upper electrode are patterned to have the same area.

22. (Original) The structure of claim 16, wherein the upper electrode is patterned to have a smaller area than that of each of the lower electrode and the capacitor dielectric layer.

23. (Original) The structure of claim 17, wherein the via is integrally formed with the lower electrode.

24. (Original) The structure of claim 16, further comprising an alignment key formed in the via-level intermetal dielectric so as to have the step difference to align the metal-insulator-metal capacitor.

25. (Original) The structure of claim 24, further comprising the metal layer for the lower electrode, the dielectric layer, and the metal layer for the upper electrode on the inner walls of the alignment key.

26. (Original) The structure of claim 24, further comprising a dummy interconnection in a stepped region of the alignment key.

27. (Original) The structure of claim 16, wherein the dual damascene interconnection is formed of at least one material selected from the group consisting of copper, gold, silver, tungsten, and any alloy thereof.

28. (Original) The structure of claim 17, wherein the via and the dual damascene interconnection are formed of different materials.

29. (Original) The structure of claim 16, further comprising:

a first lower metal interconnection and a second lower metal interconnection formed between the substrate and the via-level intermetal dielectric; and

an upper metal interconnection formed on and connected to the upper electrode, wherein the lower electrode is directly connected to the first lower metal interconnection, and the dual damascene interconnection is connected to the second metal interconnection.

30. (Previously Presented) The structure of claim 16, wherein the dual damascene interconnection further includes a via hole formed in the via-level intermetal dielectric.

31. (Previously Presented) The structure of claim 30, further comprising:

an upper metal interconnection positioned in a trench, wherein the trench is formed in the trench-level intermetal dielectric to expose the upper electrode.

32. (Previously Presented) The structure of claim 17, wherein the dual damascene interconnection further includes a via hole formed in the via-level intermetal dielectric.

33. (Previously Presented) The structure of claim 32, wherein the upper metal

interconnection is positioned in a trench, wherein the trench is formed in the trench-level intermetal dielectric to expose the upper electrode.

34. (Previously Presented) A dual damascene interconnection structure with a metal-insulator-metal capacitor, the structure comprising:

a via-level intermetal dielectric and a trench-level intermetal dielectric which are sequentially stacked on a substrate;

a dual damascene interconnection formed in the via-level intermetal dielectric and the trench-level intermetal dielectric;

a metal-insulator-metal capacitor formed between the via-level intermetal dielectric and the trench-level intermetal dielectric to include a lower electrode, a dielectric layer, and an upper electrode; and

an alignment key formed only in the via-level intermetal dielectric so as to have the step difference to align the metal-insulator-metal capacitor.

35. (Previously Presented) The structure of claim 34, further comprising the metal layer for the lower electrode, the dielectric layer, and the metal layer for the upper electrode on the inner walls of the alignment key.

36. (Previously Presented) The structure of claim 34, further comprising a dummy interconnection in a stepped region of the alignment key.

37. (Currently Amended) A dual damascene interconnection structure with a metal-insulator-metal capacitor, the structure comprising:

a via-level intermetal dielectric and a trench-level intermetal dielectric which are sequentially stacked on a substrate;

a dual damascene interconnection formed in the via-level intermetal dielectric and the trench-level intermetal dielectric;

a metal-insulator-metal capacitor formed between the via-level intermetal dielectric and the trench-level intermetal dielectric to include a lower electrode, a dielectric layer, and an upper electrode, the lower electrode being formed on the via-level intermetal dielectric; and

a first lower metal interconnection formed between the substrate and the via-level intermetal dielectric,

wherein the lower electrode extends through the via-level intermetal dielectric and is directly connected to the first lower metal interconnection.

38. (Cancelled)

39. (Cancelled)